REMARKS

Reconsideration of the application as amended is respectfully requested. Claims 1-10 remain pending.

Double Patenting Rejection

Claims 1-10 have been rejected under nonstatutory doctrine of double patenting over claims 1, 6, 11, and 12 of US Pat. No. 5,566,122. Claims 1-4 have been similarly rejected over claims 1-6 and 8-10 of US Pat. No. 6,111,775.

The terminal disclaimer submitted herewith overcomes the Examiner's double patenting rejection.

Rejections under 35 USC §102(b)

Claims 10-20 have been rejected under 35 USC §102(b) over Amitai (US 4,797,850).

Amitai discloses a dynamic random access memory controller 26 on a single chip (col 2 lines 36-37) for accessing an individual byte of data from a word of data (see the Abstract). FIG. 3 of Amitai depicts elements 12a-12d which Amitai describes as "an array of memory banks" (col 3 line 14) and further refers to the invention being capable of driving "eight banks of DRAMs" (col 5 line 44). Amitai depicts four units in each of 12a-12d of FIG. 3. Thus it appears that the term "bank" as used by Amitai refers to a plurality of individual semiconductor dice, and each of 12a-12d and 20a-20d comprises a plurality of semiconductor devices.

Further, Amitai at FIG. 5 and at col 5 lines 44-46 discloses that "RAS control signals are used to select a pair of banks, and the two CAS outputs enable the selection of one bank of the pair." Amitai also discloses at col 5 lines 48-50 that "In a 16 bit wide memory array...the RAS signals select the banks while the CAS signals select the bytes."

It thus appears that a byte of data, which is the smallest unit addressable by the invention of Amitai, is obtained from a plurality of individual DRAM devices. At the time of the filing of Amitai (1986) x8 DRAM die (die having eight data outputs, "DQs") were not produced. Amitai does not appear to discuss devices having eight or more DQs *per die*, and absent any teaching the reference cannot be assumed to refer thereto. Amitai consistently refers to accessing an individual byte of memory from a multiple byte data word, but never refers to accessing a single device or chip to obtain the byte of data. The controller itself, which is the focus of the invention, is formed on a single chip.

The claims as amended comprise novel and nonobvious differences over the disclosure of Amitai. For example, claim 1 recites "a plurality of memory dice, each memory die having at least two sub-arrays...individually addressing each sub-array of each said memory die by communicating an address to that sub-array across an address bus coupled to all said memory dice, and by individually selecting said individual memory die from among said plurality of memory dice, while the remainder of said memory dice except said individual memory die remain in a standby mode."

It appears that each of 20a-20d comprises a plurality of memory dice, not only one memory die in each of 20a-20d. In support of this, FIG. 3 depicts RAS0 alone connecting with what appear to be four separate semiconductor dice in what Amitai refers to as a "memory bank" 12a. Thus each RAS signal connects with four individual dice, and Amitai appears to indicate that its use of "memory bank" refers to a plurality of dice within one bank. FIG. 5 depicts four RAS outputs, RAS0-3, going to 20a alone. Thus 20a apparently comprises 16 memory dice, as each RAS output leads to four dice as depicted in FIG. 3. In this case 20a, which comprises 16 dice, would form two bytes of data with one bit coming from each die or chip. This is also suggested by FIG. 5 which depicts two bytes, "BYTE0" and "BYTE1" coupled with bank 20a. BYTE0 is accessed through CAS0, and BYTE1 is accessed through CAS1.

Further evidence that each "bank" of memory comprises a plurality of DRAMs is demonstrated by the paragraph beginning at column 5 line 60. It appears that using any of the DRAMs Amitai describes as being supported, a plurality of DRAMs would have to be accessed to obtain the $2x10^6$ words (16 million bits for an 8-bit word) capable of being addressed.

Thus Amitai is not capable of at least the claimed method comprising "individually selecting said individual memory die from among said plurality of memory dice, while the remainder of said memory dice except said individual memory die remain in a standby mode.

Claim 2 is further allowable over Amitai under 35 USC §102(b), at least because Amitai fails to teach or suggest a memory module.

Claim 4 is allowable over Amitai which fails to teach or suggest "addressing every sub-array of said selected memory die... and accessing one memory cell in every sub-array of only said selected memory die." As Amitai comprises multiple dice in each bank of memory to obtain a byte of data, with a byte being the smallest addressable unit, it does not appear possible for Amitai to access "every sub-array of only said selected memory die."

Claim 6 is further allowable over Amitai, which fails to teach or suggest "decoding a plurality of activation signals to determine the memory die to be individually selected."

Claim 7 is further allowable over Amitai, which fails to teach or suggest "addressing a number of memory dice from said plurality of memory dice and enabling only one die from said plurality of memory dice to access a number of data bits from only said selected memory die.

Claim 8 is allowable over Amitai, at least because Amitai fails to teach or suggest "providing a plurality of memory dice [and] coupling a plurality of data lines to each memory die, with each data line coupled to only one sub-array in each memory die." FIG. 7 of Amitai and the accompanying text at col. 5 lines 30-50 references 16 data lines (D0-D15), but it is not apparent that Amitai couples the plurality of data lines to each memory die, at least because multiple chips are accessed to obtain each byte of data as described above.

Claim 9 is further allowable under 35 USC §102(b) over Amitai, which fails to teach or suggest that the memory dice are physically coupled to a memory module.

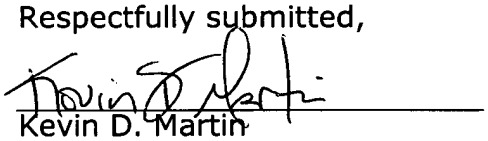
Newly added claims 11-13 are allowable over Amitai, which fails to teach or suggest providing a memory die which supplies a parity bit.

Each of the claims not individually addressed are allowable at least because they depend from an allowable claim. For at least the reasons stated above, each of claims 1-13 are allowable over the cited art.

Conclusion

Reconsideration of the application as amended is respectfully requested. If there are any matters which may be resolved or clarified through a telephone call, the Examiner is cordially invited to contact the undersigned. This is believed to be a complete response to the Examiner's office action.

Respectfully submitted,



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